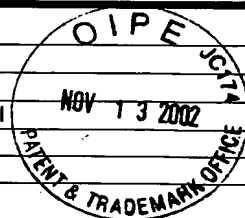


Substitute for form 1449B/PTO				Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Application Number	09/963,735
Date Submitted: November 13, 2002				Filing Date	09-27-2001
(use as many sheets as necessary)				First Named Inventor	Nobuo FUDANUKI
				Group Art Unit	2819
				Examiner Name	Unassigned
				Attorney Docket Number	016910-0476
Sheet	1	of	1		



U.S. PATENT DOCUMENTS						
Examiner Initials*	Cite No. ¹	U.S. Patent Document		Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
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FOREIGN PATENT DOCUMENTS								
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		Office ³	Number ⁴	Kind Code ⁵ (if known)				
he	A1	JP	1-100942		Semiconductor Integrated Circuit	04-19-1989		X
he	A2	JP	61-253831		Standard Cell Semiconductor Apparatus	11-11-1986		X

OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.) date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ⁶
he	A3	"A Versatile VLSI Design System for Combining Gate Array and Standard Cell Circuits on the Same Chip," Robert Hornung, Martine Bonneau and Bernard Waymel, IEEE 1987 Custom Integrated Circuits Conference.	

Examiner Signature		Date Considered	
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08/963,735

INFORMATION DISCLOSURE CITATION

(Use several sheets if necessary)

APPLICANT
FUDANUKI ET AL.

FILING DATE
12/23/1997

GROUP
2819

#11
1000
8/10/03

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EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
h	4207556	6/1980	SUGIYAMA ET AL.	326	101	
	4750027	6/1988	ASAMI	326	101	
	4809029	2/1989	MATSUMURA ET AL.	364	926	
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FOREIGN PATENT DOCUMENTS

	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
						YES	NO

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

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